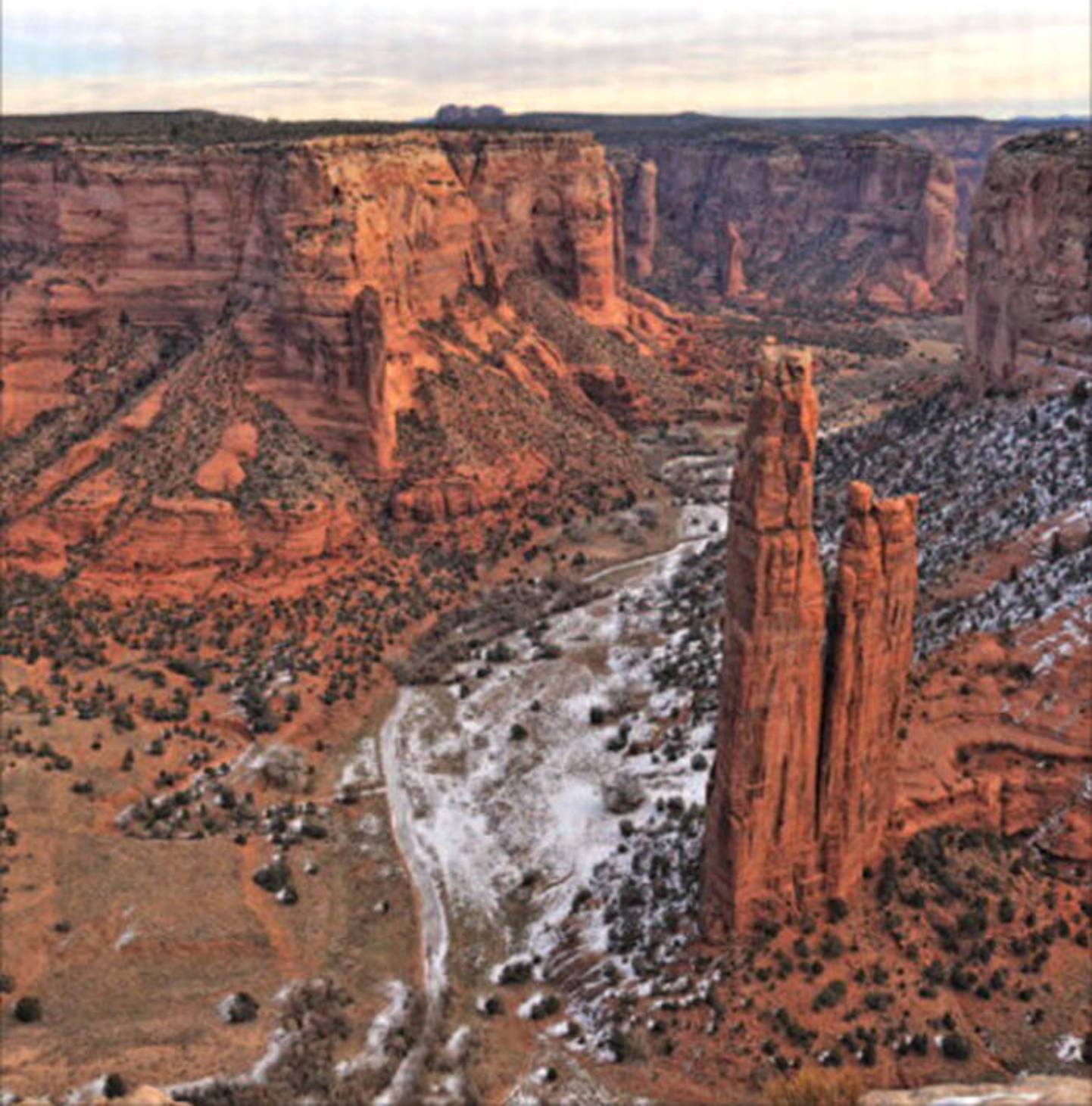
DIGITAL DESIGN

With An Introduction to the Verilog HDL

FIFTH EDITION

M. MORRIS MANO | MICHAEL D. CILETTI



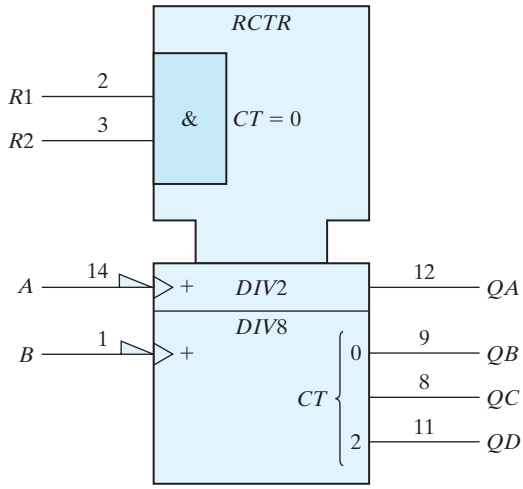


FIGURE 10.13
Graphic symbol for ripple counter, IC type 7493

the symbol $CT = 0$. Since the count input does not go to the clock inputs of all flip-flops, it has no $C1$ label and, instead, the symbol + is used to indicate a count-up operation. The dynamic symbol next to the + together with the polarity symbol along the input line signify that the count is affected with a negative-edge transition of the input signal. The bit grouping from 0 to 2 in the output represents values for the weights to the power of 2. Thus, 0 represents the value of $2^0 = 1$ and 2 represents the value $2^2 = 4$.

The standard graphic symbol for the four-bit counter with parallel load, IC type 74161, is shown in Fig. 10.14. The qualifying symbol for a synchronous counter is *CTR* followed by the symbol *DIV*16 (divide by 16), which gives the cycle length of the counter. There is a single load input at pin 9 that is split into the two modes, $M1$ and $M2$. $M1$ is active when the load input at pin 9 is low and $M2$ is active when the load input at pin 9 is high. $M1$ is recognized as active low from the polarity indicator along its input line. The count-enable inputs use the G dependencies. $G3$ is associated with the T input and $G4$ with the P input of the count enable. The label associated with the clock is

$$C5/2, 3, 4 +$$

This means that the circuit counts up (the + symbol) when $M2$, $G3$, and $G4$ are active (load = 1, $ENT = 1$, and $ENP = 1$) and the clock in $C5$ goes through a positive transition. This condition is specified in the function table of the 74161 listed in Fig. 9.15. The parallel inputs have the label 1, 5*D,* meaning that the D inputs are active when $M1$ is active (load = 0) and the clock goes through a positive transition. The output carry is designated by the label

$$3CT = 15$$

This is interpreted to mean that the output carry is active (equal to 1) if $G3$ is active ($ENT = 1$) and the content (CT) of the counter is 15 (binary 1111). Note that the outputs

7.7 **(a)** 7×128 decoders, 256 AND gates **(b)** $x = 46; y = 112$

7.8 **(a)** 8 chips **(b)** 18; 15 **(c)** 3×8 decoder

7.10 0001 1011 1011 1

7.11 101 110 011 001 010

7.12 **(a)** 0101 1010; **(b)** 1100 0110; **(c)** 1111 0100

7.13 **(a)** 6 **(b)** 7 **(c)** 7

7.14 **(a)** 0101010

7.16 24 pins

7.20 Product terms: $yz', xz', x'y'z, xy', x'y, z$

7.25 $A = yz' + xz' + x'y'z$

$B = x'y' + yz + y'z'$

$C = A + xyz$

$D = z + x'y$

CHAPTER 8

8.1 **(a)** The transfer and increment occur concurrently, i.e., at the same clock edge. After the transfer, *R2* holds the contents that were in *R1* before the clock edge, and *R2* holds its previous value incremented by 1.
(b) Decrement the content of *R3* by one.
(c) If ($S_1 = 1$), transfer content of *R1* to *R0*. If ($S_1 = 0$ and $S_2 = 1$), transfer content of *R2* to *R0*.

8.7 RTL notation:

S0: Initial state: if (start = 1) then ($RA \leftarrow$ data_A, $RB \leftarrow$ data_B, go to *S*1).
S1: $\{$Carry, $RA\} \leftarrow RA +$ (2's complement of RB), go to *S*2.
S2: If (borrow = 0) go to *S0*. If (borrow = 1) then $RA \leftarrow$ (2's complement of RA), go to *S*0.